IN THE CLAIMS

Claims 1-38 (Canceled).

39 (Previously Presented). A memory comprising:

a pair of adjacent cells having separate floating gates;

a field oxide between said cells;

a first dielectric covering said floating gates and said field oxide;

a second dielectric over said first dielectric between said floating gates, said second dielectric having a lower dielectric constant than said first dielectric; and

a control gate over said first and second dielectrics.

40 (Previously Presented). The memory of claim 39 wherein said second dielectric has a dielectric constant less than 3.9.

41 (Previously Presented). The memory of claim 39 wherein said first dielectric includes a nitride.

42 (Previously Presented). The memory of claim 41 wherein said first dielectric includes ONO.

43 (Previously Presented). The memory of claim 39 wherein said memory is a FLASH memory.

44 (Previously Presented). The memory of claim 39 wherein said second dielectric is formed by a silicon oxide layer doped with fluorine.

45 (Previously Presented). The memory of claim 39 wherein said second dielectric includes carbon.

46 (Previously Presented). The memory of claim 39 including a region between the floating gates and under said control gate, said region entirely filled by said first and second dielectrics.